WHAT IS CLAIMED IS:

1. An integrated circuit wafer comprising:

a wafer comprising a substrate comprising a wafer material, said substrate having first and second surfaces, said first surface having a circuit layer comprising integrated circuit elements constructed thereon;

a plurality of vias extending a first distance from said first surface of said substrate into said substrate from said first surface, said vias comprising a stop layer comprising a stop material that is more resistant to chemical/mechanical polishing (CMP) than said wafer material.

2. The integrated circuit wafer of Claim 1 wherein said stop material comprises a material chosen from the group consisting of Ta, TaN, W, WN, $Ta_xSi_yN_z$, W_2, and Si_yN_z, and wherein said wafer material comprises silicon.

3. The integrated circuit wafer of Claim 1 wherein said vias are lined with a layer of an electrically insulating material.

4. The integrated circuit wafer of Claim 3 wherein said electrically insulating material comprises SiO_2.

5. The integrated circuit wafer of Claim 3 wherein said vias are filled with an electrically conducting material.

6. The integrated circuit wafer of Claim 5 wherein said electrically conducting material comprises an element chosen from the group consisting of copper, tungsten, platinum, and titanium.

7. The integrated circuit wafer of Claim 1 further comprising:

a dielectric layer having top and bottom surfaces, said dielectric layer covering said circuit layer such that said bottom surface is in contact with said integrated circuit

layer; and

a plurality of electrical conductors buried in said dielectric layer and making electrical connections to said integrated circuit elements.

8. The integrated circuit wafer of Claim 7 wherein at least one of said vias extends through said dielectric layer and wherein said one of said vias is filled with an electrically conducting material, said via terminating in an electrically conducting pad on said top surface of said dielectric layer.

9. The integrated circuit wafer of Claim 8 wherein said electrically conducting pad extends above said top surface of said dielectric layer.

10. The integrated circuit wafer of Claim 8 wherein one of said electrical conductors is connected electrically to said one of said vias.

11. A method for thinning a wafer to provide a circuit layer having a predetermined thickness, said method comprising:

providing a wafer having first and second surfaces comprising a wafer material with said circuit layer fabricated on said first surface thereof;

generating a plurality of vias, each via extending from said first surface to a first depth;

depositing a layer of a stop material in said vias, said stop material being more resistant to CMP than said wafer material; and

removing material from said second surface of said wafer utilizing CMP, said layer of stop material preventing said CMP from removing wafer material closer to said first surface than said first depth.

12. The method of Claim 11 wherein said stop material comprises a material chosen from the group consisting of Ta, TaN, W, WN and wherein said wafer

material comprises silicon.

13. The method of Claim 11 wherein said wafer further comprises a layer of dielectric material covering said circuit layer, said dielectric layer being characterized by a thickness, and wherein said first distance and said thickness are equal to said predetermined thickness.

14. A method for adding a second circuit layer to a first wafer comprising a first circuit layer, said method comprising the steps of:

providing a plurality of bonding pads on a first surface of said first wafer;

providing a second wafer comprising a substrate of a wafer material and said second circuit layer, said second circuit layer being fabricated on a first surface of said substrate and being covered by a layer of dielectric material, said wafer further comprising a plurality of vias extending a predetermined distance from said first surface of said substrate into said substrate, said vias including a layer of stop material, said stop material being more resistant to CMP than said wafer material;

providing a plurality of bonding pads on said second wafer, there being a one to one correspondence between said bonding pads on said first and second wafers;

positioning said first and second wafers such that said bonding pads on said first wafer are brought in contact with said bonding pads on said second wafer;

causing said corresponding bonding pads to bond to one another; and

removing a portion of said second wafer by CMP of the surface of said second wafer that is not bonded to said first wafer, said stop layer in said vias determining the amount of material that is removed.

15. The method of Claim 14, wherein said stop material comprises a material chosen from the group consisting of Ta, TaN, W, WN and wherein said wafer material comprises silicon.

16. The method of Claim 14 further comprising the steps of:

depositing a layer of dielectric on said surface of said second wafer from which said portion was removed; and

positioning a mask with respect to said second wafer utilizing said vias as fiduciary marks.